

Chapter 5 continued – The system board

RISC vs. CISC

Instruction set.

```
0AF8:0126 007405  ADD  [SI+05],DH
0AF8:0129 80FE3A   CMP  DH,3A
0AF8:012C 7402    JZ   0130
0AF8:012E B240    MOV  DL,40
0AF8:0130 80CA20    OR   DL,20
0AF8:0133 80EA60    SUB  DL,60
0AF8:0136 E874E4    CALL E5AD
0AF8:0139 7306    JNB  0141
0AF8:013B E87FDB    CALL DCBD
0AF8:013E E9ADD8    JMP  D9EE
0AF8:0141 8BD5    MOV  DX,BP
0AF8:0143 83C205  ADD  DX,+05
```

<http://www.penguin.cz/~literakl/intel/intel.html>
144 instructions + 57 MMX +

CPU Slots and Sockets & Chipsets

CPU - AMD Athlon™ 64 Socket 939
CPU - AMD Athlon™ 64/Sempron™ Socket 754
CPU - AMD Athlon™ XP/Sempron™ Socket 462
CPU - AMD Opteron™/Athlon™ 64 FX Skt 940n

CPU - Intel® Celeron® D Socket 478
CPU - Intel® Celeron® M Socket 478
CPU - Intel® Celeron® Socket 478
CPU - Intel® Pentium® 4 Socket 478
CPU - Intel® Pentium® 4 Socket 775
CPU - Pentium M Socket 478

RISC vs. CISC

Instruction set.

```
0AF8:0126 007405  ADD  [SI+05],DH
0AF8:0129 80FE3A   CMP  DH,3A
0AF8:012C 7402    JZ   0130
0AF8:012E B240    MOV  DL,40
0AF8:0130 80CA20    OR   DL,20
0AF8:0133 80EA60    SUB  DL,60
0AF8:0136 E874E4    CALL E5AD
0AF8:0139 7306    JNB  0141
0AF8:013B E87FDB    CALL DCBD
0AF8:013E E9ADD8    JMP  D9EE
0AF8:0141 8BD5    MOV  DX,BP
0AF8:0143 83C205  ADD  DX,+05
```

<http://www.penguin.cz/~literakl/intel/intel.html>
144 instructions + 57 MMX +

Dynamic Memory & Static Memory

Levels of Cache

L1 cache is internal cache that is within the processor.

L2 cache in older systems is external cache that is normally added through an expansion slot on the system board. L2 cache on newer systems is now integral to some CPU packages.

Buses and Expansion Slots

The BUS

A path on the system board that carries electrical power, control signals, memory addresses and data to different components on the board.

ISA/EISA

PCI

AGP

USB

USB 2.0

IEEE1394 (Firewire)

Chapter 6: Understanding and Managing Memory

Physical Memory

What is the difference between storage and memory?

SRAM and DRAM

DRAM

Synchronous and Asynchronous

CACHE

Level 1

Level 2

Types of DRAM

| <i>Type of memory</i> | <i>Description</i> | <i>Packaging</i> |
|------------------------|--------------------|------------------|
| Synchronous DRAM | | |
| Double data rate (DDR) | | |
| Rambus DRAM | | |
| | | |

Memory packaging.

SIMMs 30 & 72 pin

DIMMs

RIMMS

Reading Memory sizes

128MB RIMM

8x64 SDRAM

2x64 SDRAM

PC100 64MB SDRAM

PC2100 DDR

Wat is CAS Latency?

Number of clock cycles that pass while data is written.

CL2 (CAS 2)

CL3 (CAS 3)

Other types

Programmable ROM (PROM).

Erasable Programmable ROM (EPROM).

Electrically Erasable Programmable ROM (EEPROM)

Buffering

Adding Logic, particularly drivers, to a SIMM or DIMM to increase the output current

Cache

A small high speed memory device, (usually SRAM) located between the CPU and system DRAM used to temporarily store data. Properly designed, a cache improves system performance by reducing the need to access the system's main memory for every transaction. Cache memory can be three to five times faster than standard system DRAM.

CPU

Central Processing Unit. The computer chip primarily in charge of retrieving, decoding and executing instructions.

DIMM

Dual Inline Memory Modules. DIMMs are memory modules with data buses of 64, 72 or 80 bits.

DRAM

Dynamic Random Access Memory

ECC

Error Correction Code, is an electronic method for checking the integrity of data stored in DRAM. ECC is more elaborate than parity since it can detect multiple bit errors and can locate and correct single bit errors. ECC usually uses three bits per byte of data, compared to one bit used on parity.

EDO

Extended Data Output, A DRAM performance feature that speeds up the read cycle between the CPU and memory. Made for computers with a faster CPU, EDO memory is 10-15% faster than similar fast-page mode chips.

FPM

Fast t Page Mode – Common DRAM data access mode that is similar to finding information in an encyclopedia. First, you turn to a specific page, then you select information from the page.

JEDEC

Joint Electronic Device Engineering Council is the consortium of manufacturers that devises standards most notably for computer memory modules. Industry standard memory usually implies compliance with a particular group of JEDEC standards.

Nanosecond

ns, One billionth of a second. Times for memory data access are measured in nanoseconds

Parity

A method of data integrity checking that adds a single bit to each byte of data. The parity bit is responsible for checking for errors in the other 8 bits. Unlike ECC, parity only detects but doesn't correct errors.

PCMCIA

Personal Computer Memory Card International Association, A created standard to allow interchangeability, of various computer components such as; memory, FAX/modem, SCSI, and networking products all on the same connector.

SDRAM

Synchronous Dynamic Random Access Memory, A DRAM designed to deliver bursts of data at very high speed using automatic addressing, multiple page interleaving, and a synchronous (or clocked) interface.

SIMM

Single In-line memory Module are narrow printed circuit boards about three inches long that hold several memory chips. The module plugs into a SIMM socket on the main or expansion board of your computer or printer.

What are system Resources.....

| Resource- | Windows 3.1 | Windows 95/98/ME | Windows NT/2000/XP |
|---------------------------------|---------------------|-------------------------|---------------------------|
| Window/Menu Handles | about 200 | 32KB (each) | Unlimited |
| Timers | 32 | Unlimited | Unlimited |
| COM/LPT ports | 4 each | Unlimited | Unlimited |
| Listbox items (per listbox) | 8KB | 32KB | Unlimited |
| Listbox data (per listbox) | 64KB | Unlimited | Unlimited |
| Edit control data (per control) | 64KB | Unlimited | Unlimited |
| Regions | All in 64KB segment | Unlimited | Unlimited |
| Logical pens, brushes | All in 64KB segment | 64KB segment | Unlimited |
| Physical pens, brushes | All in 64KB segment | Unlimited | Unlimited |
| Logical fonts | All in 64KB segment | 750-800 | Unlimited |
| Installed fonts | 250-300 (best case) | 1000 | Unlimited |
| Device Contexts | 200 (best case) | 16KB | Unlimited |